CLAIMS

1. A digital rate converter comprising:

a first interpolator including an input, the input receiving a data signal at a first sampling rate, the first sampling rate is based on a first clock signal, the first interpolator having an output to provide a data signal at a second sampling rate, the second sampling rate being greater than the first sampling rate as per an upsampling factor;

a buffer including a plurality of buffer positions and an input coupled to the output of the first interpolator to receive the data signal provided by the output;

selection circuitry coupled to the buffer;

a second interpolator coupled to the selection circuitry, the selection circuitry providing values of a subset of buffer positions of the plurality of buffer positions to the second interpolator dependent on a position indicator, the second interpolator having a data output for providing a data output signal at a third sampling rate, the third sampling rate is based on a second clock signal, wherein the first clock signal and the second clock signal are independent of each other, wherein the output of the second interpolator provides an output value dependent upon a fractional indicator; and

a digital sampling positioner, the digital sampling positioner including a first output for providing the position indicator and a second output for providing the fractional indicator.

2. The converter of claim 1 wherein the first sampling rate is lower than a frequency of the first clock signal and the third sampling rate is lower than a frequency of the second clock signal.

3. The converter of claim 1 wherein the digital sampling positioner has a first input for receiving the first clock signal and a second input for receiving the second clock signal, wherein the position indicator and the fractional indicator are dependent upon the first clock signal and the second clock signal.

4. The converter of claim 1 wherein the subset of buffer positions are consecutive buffer positions of the plurality.

5. The converter of claim 1 wherein the second interpolator is a Lagrange interpolator.

6. The converter of claim 1 wherein the subset of buffer positions includes 5 buffer positions.

7. The converter of claim 1 wherein the fractional indicator is dependent upon a previous value of the fractional indicator.

8. The converter of claim 1 wherein the position indicator is dependent upon a previous value of the position indicator.

9. The converter of claim 1 wherein the third sampling rate is in a range of approximately .5 times the second sampling rate to approximately 1.5 times the second sampling rate.

10. The converter of claim 1 wherein the second clock signal is at approximately 48 megahertz.

11. A digital amplifier including the digital rate converter of claim 1 and further comprising:

a pulse width modulated (PWM) digital amplifier including an input coupled to the output of the second interpolator.

12. The digital amplifier of claim 11 wherein the digital amplifier has an output synchronous with the second clock signal.

13. The converter of claim 1 wherein the upsampling factor is based upon a ratio of the first sampling rate and the third sampling rate.

14. The converter of claim 1 wherein first interpolator includes an input to receive an upsampling signal, the upsampling factor is based on the upsampling signal.

15. The converter of claim 1 wherein the output of the second interpolator provides an output value that is an interpolated value offset from a buffer position of the subset of buffer positions, wherein the offset is dependent upon the fractional indicator.

16. The converter of claim 15 wherein the output value is an interpolated value offset from a center buffer position of the subset.

17. The converter of claim 1 wherein the position indicator is dependent upon a previous value of the position indicator and a previous value of the fractional indicator.

18. The converter of claim 1 wherein the fractional indicator is dependent upon a previous value of the position indicator and a previous value of the fractional indicator.

19. The converter of claim 1 wherein

the position indicator and fractional indicator are dependent upon a representation of a ratio of the second sampling rate to the third sampling rate.

20. An electronic system comprising the converter of claim 1 and further comprising:

a digital signal processor coupled to the input to provide the data input signal.

21. The converter of claim 1 wherein the converter includes a physical input, the converter receiving the data signal at the first sampling rate and the first clock signal via the physical input.

22. The converter of claim 1 wherein the position indicator and the fractional indicator are dependent upon a buffer pointer from the buffer.

23. A method of converting a data signal at an input sampling rate to a data signal at an output sampling rate in a digital rate converter, the method comprising:

upsampling the input data signal at a input sampling rate to an intermediate data signal at an intermediate sampling rate wherein the intermediate sampling rate is greater than the input sampling rate as per an upsampling factor;

storing sample values of the intermediate data signal into buffer positions of a buffer;

providing a first plurality of buffer position values from a first subset of buffer positions of the buffer to an interpolator, the buffer positions making up the first subset being dependent upon a position indicator; and

providing at the output of the interpolator a output data signal at an output sampling rate, a value of the output data signal is dependent upon a fractional indicator provided to the interpolator;

wherein the input sampling rate is based on a first clock signal and the output sampling rate is based on a second clock signal, wherein the first clock signal and the second clock signal are independent of each other.

24. The method of claim 23 wherein the input sampling rate is lower than a frequency of the first clock signal and the output sampling rate is lower than a frequency of the second clock signal.

25. The method of claim 23 wherein the position indicator and the fractional indicator are dependent upon the first clock signal and the second clock signal.

26. The method of claim 23 wherein the subset of buffer positions are consecutive buffer positions.

27. The method of claim 23 wherein the interpolator is a Lagrange interpolator.

28. The method of claim 23 wherein the subset of buffer positions includes 5 buffer positions.

29. The method of claim 23 wherein the fractional indicator is dependent upon a previous value of the fractional indicator.

30. The converter of claim 23 wherein the position indicator is dependent upon a previous value of the position indicator.

31. The method of claim 23 wherein the output sampling rate is in a range of approximately .5 times the intermediate sampling rate to approximately 1.5 times the intermediate sampling rate.

32. The method of claim 23 wherein said output data signal is input into a pulse width modulated (PWM) digital amplifier.

33. The method of claim 32 wherein said data signal that is input into said pulsed width modulated digital amplifier is synchronous with the second clock signal.

34. The method of claim 23 further comprising:
adjusting the upsampling factor to accommodate a change in the input sampling rate.

35. The method of claim 23 wherein value of the output data signal is an interpolated value offset from a buffer position of the subset of buffer positions, wherein the offset is dependent upon the fractional indicator.

36. The method of claim 35 wherein the output value is an interpolated value offset from a center buffer position of the subset.

37. The method of claim 23 wherein the position indicator is dependent upon a previous value of the position indicator and a previous value of the fractional indicator.

38. The method of claim 23 wherein the fractional indicator is dependent upon a previous value of the position indicator and a previous value of the fractional indicator.

39. The method of claim 23 wherein:

the position indicator and fractional indicator are dependent upon a representation of a ratio of the intermediate sampling rate to the output sampling rate.

40. The method of claim 23 wherein the input data signal is provided by a digital signal processor.

41. The method of claim 23 wherein the upsampling the input data signal, the storing sample values of the intermediate data signal, the providing a first plurality of buffer position values, and the providing at the output of the interpolator are performed by a processor executing code.

42. A digital rate converter comprising:

a first interpolator including an input, the input receiving a data signal at a first sampling rate, the first sampling rate is based on a first clock signal, the first clock signal having a frequency that is greater than the first sampling rate, the first interpolator having an output to provide a data signal at a second sampling rate, the second sampling rate being greater than the first sampling rate as per an upsampling factor;

a buffer including a plurality of buffer positions and an input coupled to the output of the first interpolator to receive the data signal provided by the output;

selection circuitry coupled to the buffer; and

a second interpolator coupled to the selection circuitry, the selection circuitry providing values of a subset of buffer positions of the plurality of buffer positions to the second interpolator dependent on a position indicator, the second interpolator having a data output for providing a data output signal at a third sampling rate, the third sampling rate is based on a second clock signal, the second clock signal having a frequency that is greater than the third sampling rate, wherein the first clock signal and the second clock signal are independent of each other, wherein the output of the second interpolator provides an output value dependent upon a fractional indicator;

a digital sampling positioner, the digital sampling positioner including a first output for providing the position indicator and a second output for providing the fractional indicator, wherein the position indicator and the fractional indicator are dependent upon a previous value of the position indicator and a previous value of the fractional indicator.